CLAIMS:

Claims 1 and 16 have been amended. No claims have been added or canceled herein. This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A method for manufacturing an interconnect for an integrated circuit, comprising:

forming a surface conductive lead in an opening formed within a protective overcoat and over a barrier layer, the barrier layer providing additional adhesion between the protective overcoat and the surface conductive lead, a portion of the barrier layer extending beyond the surface conductive lead;

providing a seed layer directly contacting the barrier layer and at least partially within the opening of the protective overcoat;

subjecting the seed layer to a wet etch, wherein the wet etch is without substantially undercutting the etched seed layer or surface conductive lead and without substantially affecting the barrier layer;

subjecting the portion of the barrier layer to a dry etch, subsequent to subjecting the seed layer to a wet etch, to remove the portion and form a skirt, the dry etch selective to the barrier layer without substantially undercutting the etched seed layer or surface conductive lead, without width reduction of the surface conductive lead, and without oxide formation on side walls of the surface conductive lead; ~~and~~

~~subjecting the seed layer to a wet etch prior to subjecting the portion of the barrier layer to the dry etch, wherein the wet etch is without substantially undercutting the etched seed layer or surface conductive lead~~.

2. (Previously Presented) The method as recited in Claim 1 wherein the dry etch comprises carbon tetrafluoride.

3. (Previously Presented) The method as recited in Claim 2 wherein the dry etch further comprises nitrous oxide.

4. (Previously Presented) The method as recited in Claim 2 wherein the dry etch further comprises oxygen or chlorine.

5. (Original) The method as recited in Claim 1 wherein the barrier layer is a tungsten titanium barrier layer.

6. (Original) The method as recited in Claim 1 wherein the barrier layer has a thickness ranging from about 200 nm to about 300 nm.

7. (Canceled).

8. (Previously Presented) The method as recited in Claim 1 wherein the wet etch comprises an etch chemistry comprising hydrogen peroxide and sulfuric acid.

9. (Original) The method as recited in Claim 1 wherein the surface conductive lead has a width ranging from about 3 μm to about 200 μm.

10. (Original) The method as recited in Claim 1 wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers, and silicon nitride layers, phospho-silicate glass layers, and organic polymer layers.

11. (Withdrawn) An interconnect for use in an integrated circuit, comprising:

a surface conductive lead located in an opening formed within a protective overcoat; and

a barrier layer located between the protective overcoat and the surface conductive lead, a portion of the barrier layer forming a skirt that extends outside a footprint of the surface conductive lead.

12. (Withdrawn) The interconnect recited in Claim 11 wherein the skirt that extends from about 250 nm to about 2000 nm outside the footprint.

13. (Withdrawn) The interconnect recited in Claim 11 wherein a thickness of the skirt tappers down as is moves away from the surface conductive lead.

14. (Withdrawn) The interconnect recited in Claim 11 further including a seed layer

located between the barrier layer and the surface conductive lead, wherein substantially no undercut exists in the seed layer.

15. (Withdrawn) The interconnect as recited in Claim 11 wherein the surface conductive lead has a width ranging from about 3 Φm to about 200 Φm.

16. (Currently Amended) A method for manufacturing an integrated circuit, comprising:

forming transistor devices over a semiconductor substrate;

forming one or more metallization layers over the transistor devices, the one or more metallization layers interconnecting one or more of the transistor devices;

forming a protective overcoat over the one or more metallization layers, wherein the protective overcoat has an opening located therein;

forming a surface conductive lead in the opening and over a barrier layer, the barrier layer providing additional adhesion between the protective overcoat and the surface conductive lead, a portion of the barrier layer extending beyond the surface conductive lead;

providing a seed layer directly contacting the barrier layer and at least partially within the opening of the barrier layer;

subjecting the seed layer to a wet etch, wherein the wet etch is without substantially undercutting the etched seed layer or surface conductive lead and without substantially affecting the barrier layer; and

subjecting the portion of the barrier layer to a dry etch, subsequent to subjecting the seed layer to the wet etch, to remove the portion thereby forming a skirt, the dry etch selective to the barrier layer without substantially undercutting the etched seed layer or surface conductive lead, without a width reduction of the surface conductive lead, and without oxide formation on side walls of the surface conductive lead; ~~and~~

~~subjecting the seed layer to a wet etch prior to subjecting the portion of the barrier layer to the dry etch, wherein the wet etch is without substantially undercutting the etched seed layer or surface conductive lead~~.

17. (Canceled).

18. (Previously Presented) The method as recited in Claim 16 wherein the wet etch comprises an etch chemistry comprising hydrogen peroxide and sulfuric acid.

19. (Previously Presented) The method as recited in Claim 16 wherein the surface conductive lead has a width ranging from about 3 μm to about 200 μm.

20. (Original) The method as recited in Claim 16 wherein the protective overcoat comprises one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers, and silicon nitride layers, phospho-silicate glass layers, and organic polymer layers.

21. (Previously Presented) The method as recited in Claim 1 wherein a thickness of the skirt tapers down as it moves away from the surface conductive lead.

22. (Previously Presented) The method as recited in Claim 16 wherein a thickness of the skirt tapers down as it moves away from the surface conductive lead.